

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 34, 35, 37, and 41-43. Please amend claims 32, 39, 40, and 45, and add new claims 50-52, as follows:

Listing of Claims:

1-31. (Cancelled)

32. (Currently amended) In a graphics processing system having a memory system including an embedded memory array and having error-correction coding, a [[A]] method for accessing the embedded [[a]] memory array, comprising:

reading data and an associated error correction code from a location corresponding to a memory address in the embedded memory array;

storing the data at a buffer location in a buffer memory having a plurality of buffer locations for storing a plurality of data;

storing the memory address;

processing ~~modifying~~ at least a portion of the data to provide modified data;

receiving write memory addresses; and

when writing the modified data to the embedded memory array in response to a write memory address matching the stored memory address,

logically combining the stored data and the modified data and storing the combined data at the buffer location ~~updating the data stored in the memory with the modified portion of the data;~~

calculating a new error correction code based on the combined ~~updated~~ data in the buffer memory; and

storing the combined ~~updated~~ data and the new error correction code to the location corresponding to the memory address in the embedded memory array.

33. (Currently amended) The method of claim 32 wherein processing ~~modifying~~ at least a portion of the data to provide modified data comprises performing graphics processing operations on the data.

34. (Cancelled)

35. (Cancelled)

36. (Previously presented) The method of claim 32, further comprising:
substantially concurrent with the reading and storing of data, updating second data previously stored in a second memory with a modified portion of the second data; and
substantially concurrent with the updating of the data, reading third data and storing the third data in the second memory.

37. (Cancelled)

38. (Previously presented) The method of claim 32, further comprising
providing the data read from the location to an output bus for provision to a requesting entity.

39. (Currently amended) In a graphics processing system having a memory system including an embedded memory array and having error-correction coding, a [[A]] method for accessing [[a]] the embedded memory array, comprising:

reading first data and an associated error correction code from a first location corresponding to a first memory address in the embedded memory array;

storing the first data at a first buffer location in a first buffer memory having a plurality of buffer locations for storing a plurality of data;

substantially concurrent with the reading and storing of the first data in the first buffer memory,

logically combining ~~updating~~ second data previously stored at a second buffer location in a second buffer memory with modified data;

calculating a new error correction code based on the combined updated second data in the second buffer memory; and

storing the combined updated second data and the new error correction code to a second the location corresponding to a second memory address in the embedded memory array from which the ~~original~~ second data was originally read;

processing modifying at least a portion of the first data to provide first modified data;

reading third new data from a third new location corresponding to a third memory address in the embedded memory array;

storing the third new data at a third buffer location in the second buffer memory; and

substantially concurrent with the reading and storing of the third new data, logically combining updating the first data stored at the first buffer location in the [[a]] first buffer memory with the first modified ~~portion of the first data~~;

calculating a new error correction code based on the combined updated first data in the first buffer memory; and

storing the combined updated first data and the new error correction code to the first location corresponding to the first memory address in the embedded memory array.

40. (Currently amended) The method of claim 39 wherein processing modifying at least a portion of the first data to provide first modified data comprises performing graphics processing operations on the first data.

41-43. (Cancelled)

44. (Previously presented) The method of claim 39, further comprising providing the first data to an output bus for provision to a requesting entity.

45. (Currently amended) A memory system, comprising:
an embedded memory having a read data port and a write data port;

an error-correction code (ECC) generator coupled to the write data port and configured to generate an associated ECC for data written to the embedded memory;

an ECC check circuit coupled to the read data port and configured to confirm the integrity of the data based on the associated ECC;

a memory having an output coupled to the ECC generator and further having an input coupled to the ECC check circuit, the memory configured to store data read from the embedded memory and to store a memory address associated with the stored data, the memory further configured to output the stored data associated with a memory address in response to receiving the same;

a first selection circuit having an input coupled to the output of the ~~first~~ memory, and a first output coupled to a read bus and a second output coupled to the ECC generator and the write data port;

a second selection circuit having an output, and further having a first input coupled to the ECC check circuit and a second input coupled to a write bus;

combination logic having an output coupled to the input of the memory, a first input coupled to the output of the memory and a second input coupled to the ECC check circuit, the combination logic configured to combine data applied to the first and second inputs and provide combined data at the output; and

a control circuit coupled to the first and second selection circuits, the memory, and the combination logic, the control circuit configured to control the first and second selection circuits and coordinate the storing of data from the embedded memory in the memory and provide the data to an ~~the~~ output bus, and in response to receiving a write request, coordinate the combining of modified data received from the write bus with corresponding original data previously stored in the memory and further provide the combined data for ECC calculation and writing to the memory location in the embedded memory from where the original data was read.

46. (Previously presented) The apparatus of claim 45, further comprising:

a second memory an output coupled to the ECC generator and an input coupled to the ECC check circuit, the second memory configured to store data read from the embedded memory and to store a memory address associated with the stored data, the memory further

configured to output the stored data associated with a memory address in response to receiving the same;

second combination logic having an output coupled to the second memory, a first input coupled to the output of the second memory, and a second input coupled to the ECC check circuit, the second combination logic configured to combine data applied to the first and second inputs and provide combined data at the output.

47. (Previously presented) The apparatus of claim 46 wherein the control circuit is further configured to coordinate the storing of data from the embedded memory in the second memory and provide the data to the output bus, and in response to receiving a write request, coordinate the combining of modified data received from the write bus with corresponding original data previously stored in the second memory and further provide the combined data for ECC calculation and writing to the memory location in the embedded memory from where the original data was read.

48. (Previously presented) The apparatus of claim 45 wherein the memory comprises a static random access memory.

49. (Previously presented) The apparatus of claim 45 wherein the embedded memory comprises a dual-port embedded memory.

50. (New) The method of claim 32 wherein storing the data at a buffer location in a buffer memory comprises storing the data at a buffer location in a first-in-first-out (FIFO) buffer.

51. (New) The method of claim 39 wherein storing the first data at a first buffer location in a first buffer memory comprises storing the first data at a first buffer location in a first-in-first-out (FIFO) buffer.

52. (New) The apparatus of claim 45 wherein the memory comprises a first-in-first-out (FIFO) buffer.